Submitted to Session 5 - Emerging Technologies, of the ULSI Process Integration Symposium

Synthesis and Devices of Graphene

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As CMOS devices are scaled below 65nm, high mobility channel material is desired nowadays to achieve high performance. Graphene, which is one or a few layers of graphite, has gained much interest. It is shown experimentally to have an ultra high mobility of around 15,000cm^2/Vs [1], and a large intrinsic carrier density of around 10^{12}/cm^2 [2]. Its 2-dimension nature also shows better prospects for scalable integration into planar CMOS structures. In this paper, we will discuss several methods of synthesis of graphene as well as the device performance based on transistors with graphene as a channel material.

Graphene films less than two layers thick have been successfully grown using CH_4 as a precursor on a Ni-catalyst surface by Chemical Vapor Deposition (CVD). A 300-500 nm thick nickel layer was deposited on SiO_2 substrate, and then annealed at 600-1000°C in an environment designed to control oxidation, and nickel grain structure. The nickel grain structure directly influences the uniformity, nucleation and growth of graphene films. In our experiments we find that maintaining a high ratio of H_2 to CH_4 promotes the growth of few layer graphene films on a thermal annealed Ni surface. It is found that the synthesis of less than 2 layers graphene is successfully performed from Raman spectroscopy, AFM and TEM. The graphene is then transferred on to SiO_2/Si substrate for further device fabrication.

Both back-gated and top-gated graphene channel transistors are fabricated with graphene from several different synthesis methods. The back-gated graphene channel transistor has silicon substrate served as a back-gate and high-k material is deposited on top of Si substrate as the gate dielectric. In top-gated graphene channel transistor, PECVD Oxide and Aluminum are deposited on graphene to form top-gate stack. Both Metal and PolySi are used as source and drain materials.

Graphene channel transistors with metal source/drain show an ambipolar conduction, which can be clearly seen from I_D-V_G curves. This is because of large density of both electrons and holes in graphene [1]. However, for the transistor with p-type PolySi in source and drain, drain current decreases with increasing gate voltage, which indicates a hole conduction through the transistor; and for the transistor with n-type PolySi source and drain, drain current increases with increasing gate voltage, which on the other hand indicates an electron conduction. This proves the concept that the Schottky junctions formed at source/drain allow only one kind of carriers to conduct in graphene [3].

In summary, method of synthesis graphene is described and 1-2 layers of graphene is successfully realized which is identified by Raman Spectroscopy, AFM and TEM. Both back-gated and top-gated graphene channel transistors are demonstrated. With metal source/drain, the transistor has ambipolar conduction while with PolySi applied at source/drain, the conduction becomes unipolar, which proves one kind of carriers conduction along the channel. Therefore the transistor with graphene channel will maintain high current but be better turned off.

Reference

[1] S.V.Morozov et al, Phys.Rev.B, 72, (2005)
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[3] Jing Zhu et al, ESSDERC, (2007)

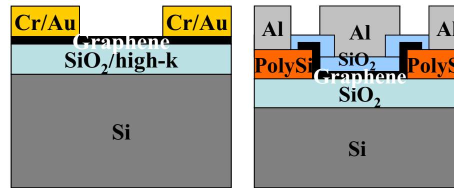

Figure 1. Schematics of Graphene Channel Transistors. Left hand is Back-gated Graphene Channel Transistor with Metal Source and Drain. Right hand is Top-gated Graphene Channel Transistor with PolySi Source and Drain.

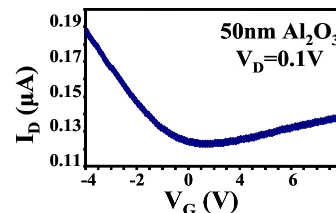

Figure 2. I_D-V_G Characteristics of Graphene Channel Transistors with Metal Source and Drain

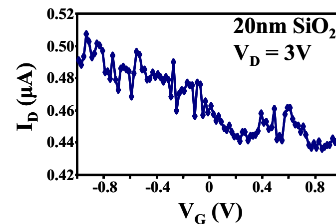

Figure 3. I_D-V_G Characteristics of Graphene Channel Transistors with P-type PolySi Source and Drain

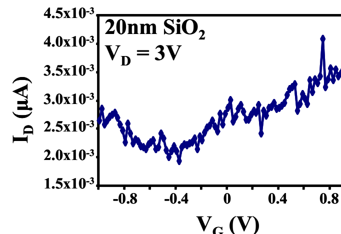

Figure 4. I_D-V_G Characteristics of Graphene Channel Transistors with N-type PolySi Source and Drain